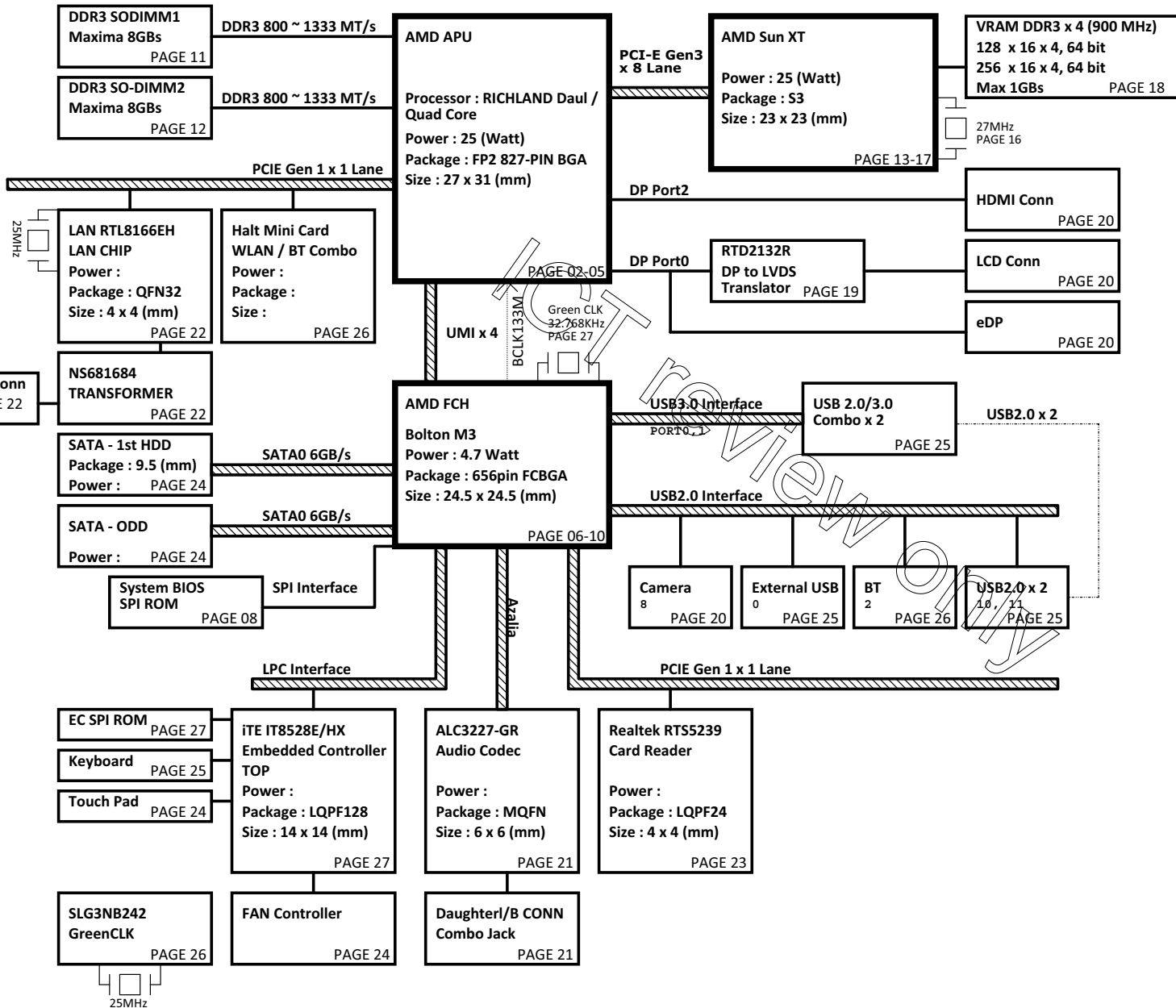


# Perrier\_AMD RICHLAND DIS/UMA (14"/15.6")



## PCB 6L STACK UP

LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1(High)  
LAYER 4 : IN2(Low)  
LAYER 5 : SVCC  
LAYER 6 : BOT

## Power Source

BQ24728  
System Charge Power (+BATCHG)

G5934RZ1U  
System Discharge Power  
(+1.5V/+3V/+5V)  
(+3VSUSV/+3VLAVCC/+1.1V)

Ricktek RT8223PZ  
System Power (+3VPCU/+5VPCU/  
+3VS5/+5VS5)

SL6277/RT8228AZ/AP3407A/ISL6208BCRZ  
Processor Power (+VCC\_CORE/  
+1.2V/+2.5V/+VDDNB\_CORE)

TP551216RUKR  
System Memory Power (+1.5VSUS/  
+0.75V\_DDR\_VTT)

AOZ1237QI-02  
PCH Power (+1.1VS5)

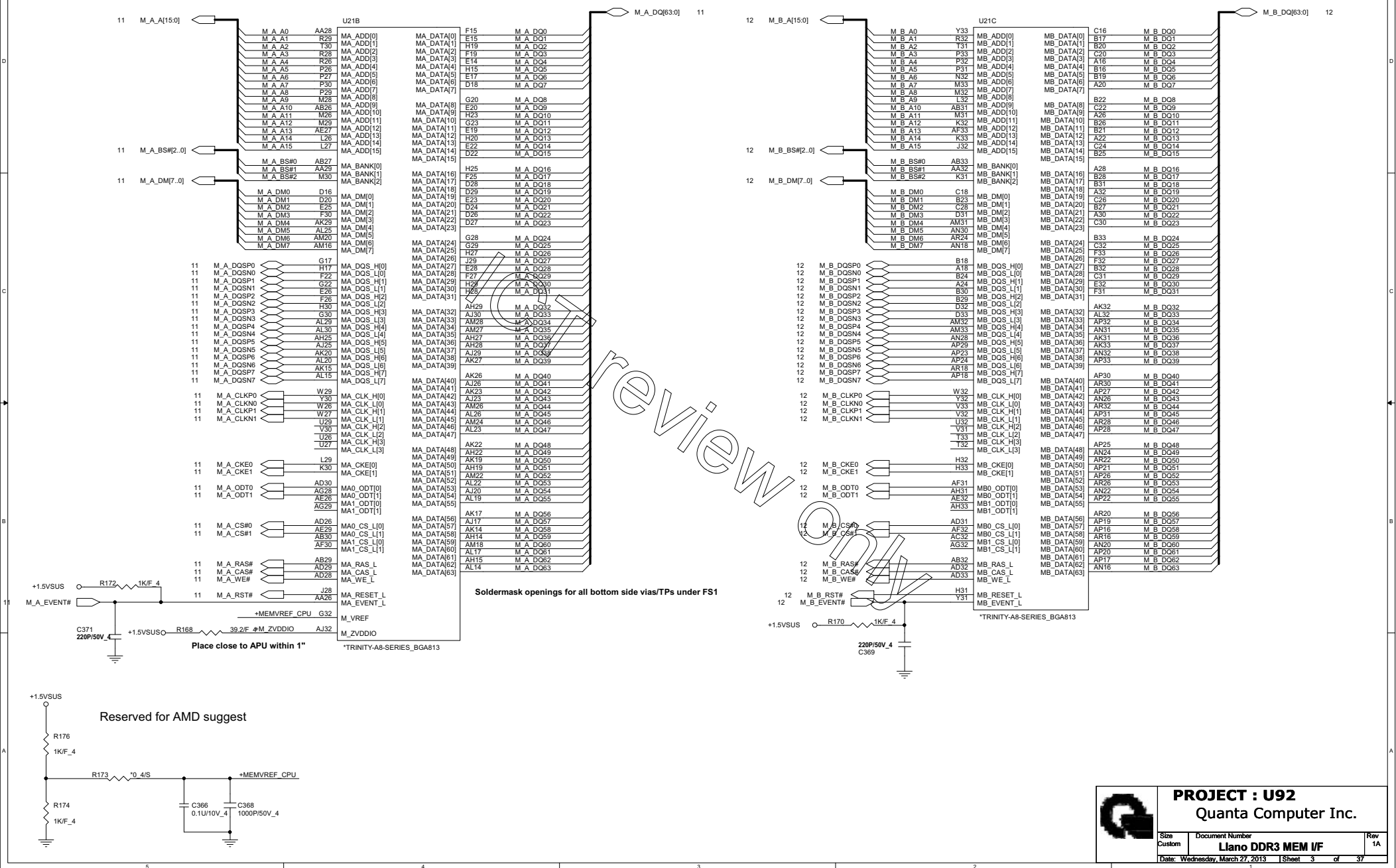
ADP3211A  
DGPU Power (+VGA\_CORE/+1.0V\_VGA/+3V\_VGA/  
+1.5V\_VGA/+1.8V\_VGA/+VDDCI)



**PROJECT : U92**  
Quanta Computer Inc.

Size A3	Document Number Block Diagram	Rev 1A
Date: Wednesday, March 27, 2013	Sheet	1 of 37



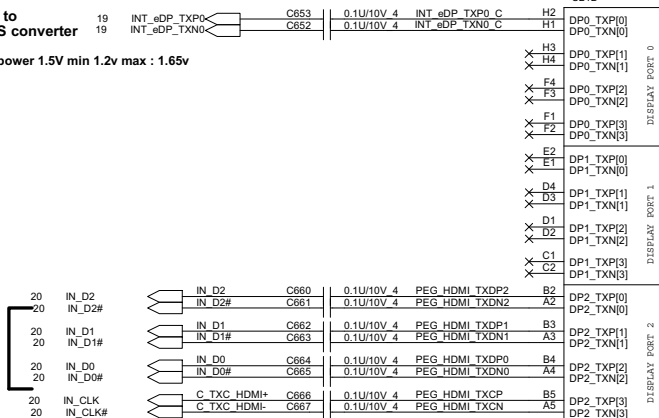


**PROJECT : U92**  
Quanta Computer Inc.

Size Custom	Document Number <b>Llano DDR3 MEM I/F</b>	Rev 1A
Date: Wednesday, March 27, 2013 Sheet 3 of 37		

DP0 output to  
eDP to LVDS converter

**Display port power 1.5V min 1.2v max : 1.65v**



**4/19 HDMI change to DP2 for Comal.**

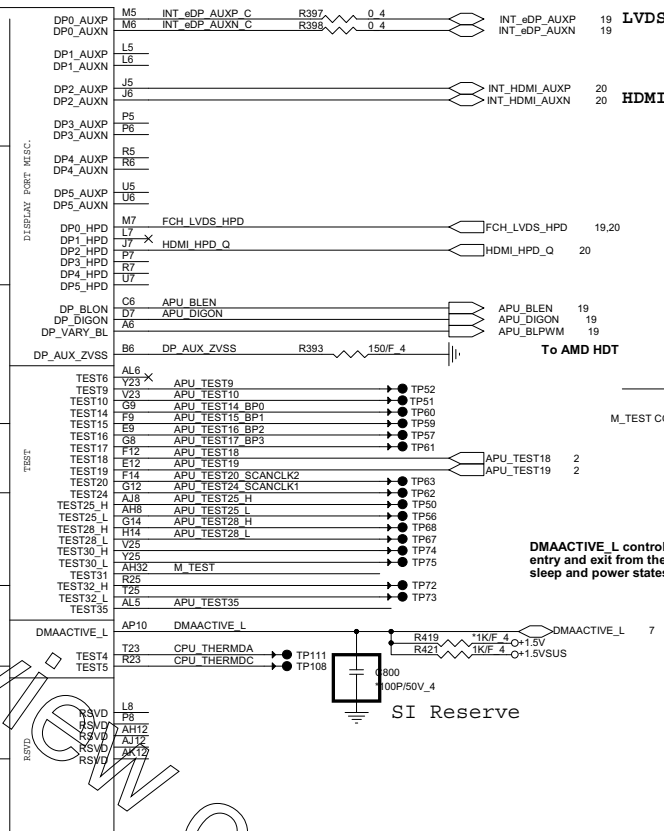
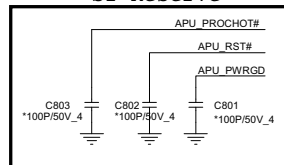
**DP2 output to  
HDMI connector**

note --HDMI P&N can not swap

Note: CLK\_APU\_HCLKP/N is 100MHZ SSC

Note: CLK DP NSSCP/N is 100MHZ non-SSC

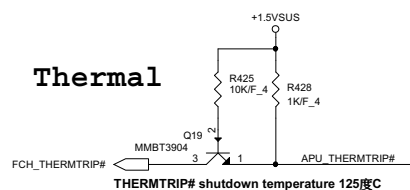
SI Reserve



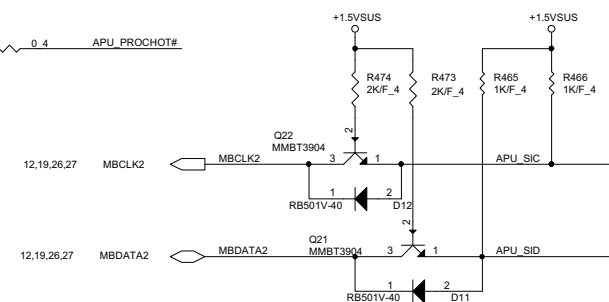
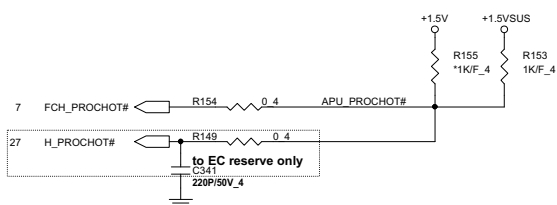
**DMAACTIVE\_L** controls entry and exit from the sleep and power states

SI Reserve

## Thermal



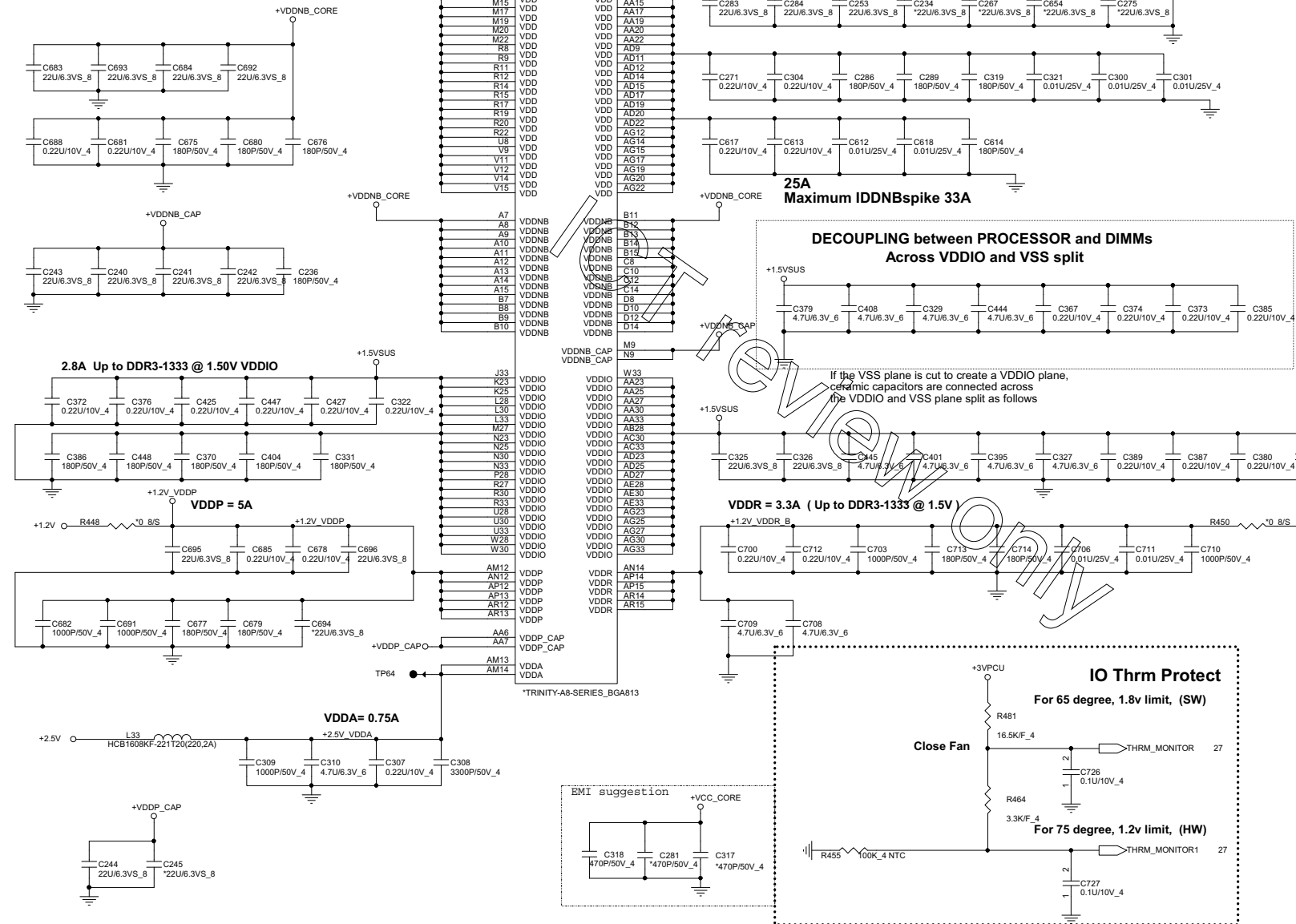
9 For Comal,  
se to APU.



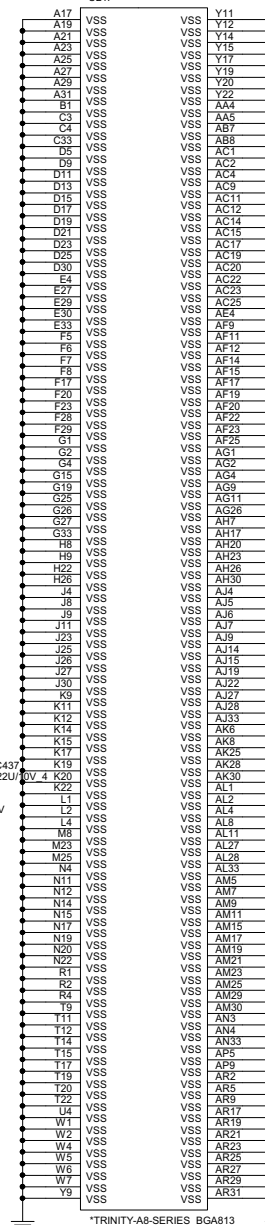
Size	Document Number	R
	<b>Llano Display/Misc</b>	
Date:	Wednesday, March 27, 2013	Sheet 4 of 37

APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



U21F

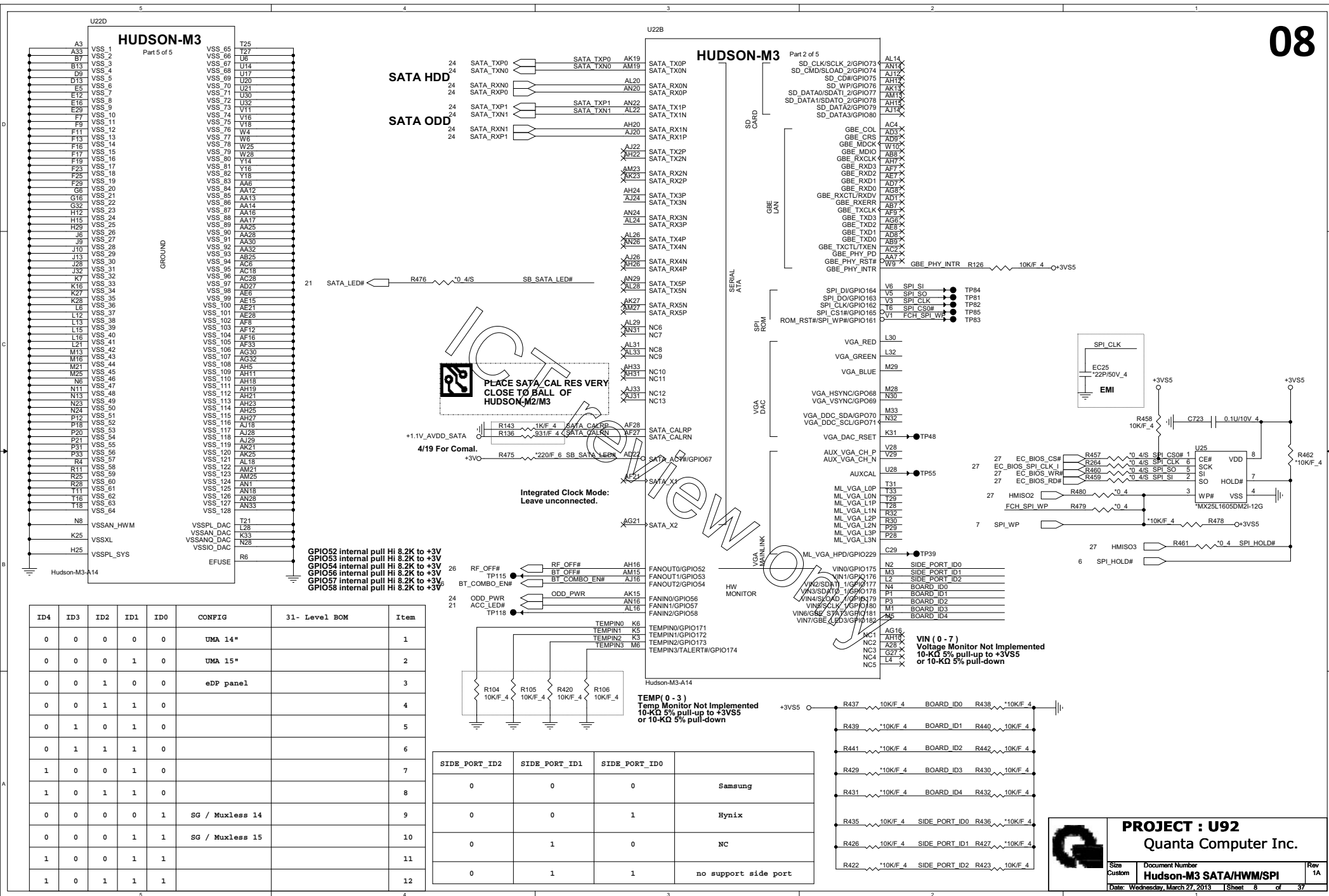


**PROJECT : U92**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	Llano POWER/GND	1A
Date: Wednesday, March 27, 2013	Sheet 5 of 37	







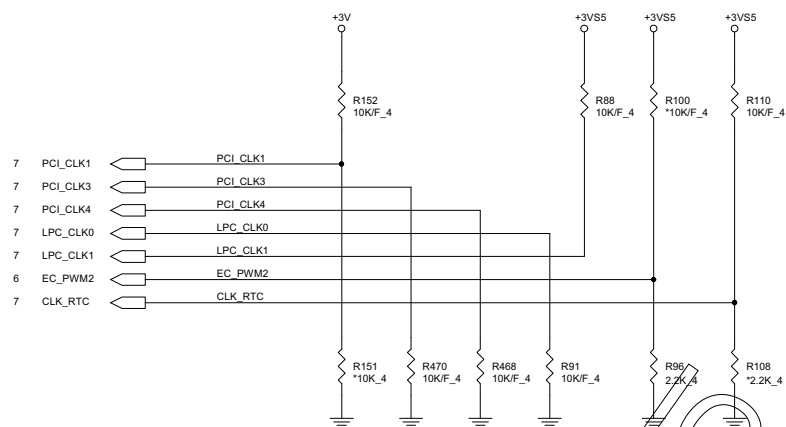




## STRAPS PINS



OVERLAP COMMON PADS WHERE  
POSSIBLE FOR DUAL-OP RESISTORS.

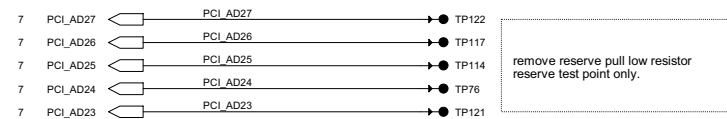


## REQUIRED STRAPS

		PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	*****	ALLOW PCIe Gen2  DEFAULT	*****	USE DEBUG STRAP	non_Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED  DEFAULT	S5 PLUS MODE ENABLED  DEFAULT
PULL LOW	*****	FORCE PCIe Gen1	*****	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED  DEFAULT	S5 PLUS MODE DISABLED

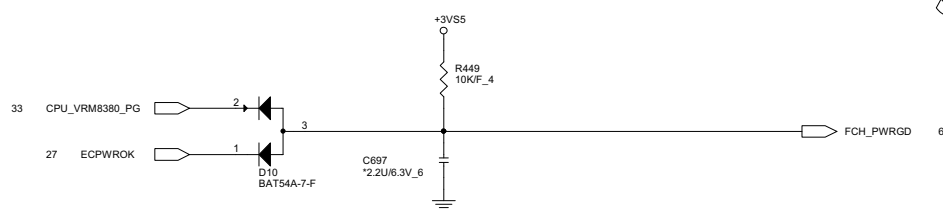
## DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI\_AD[27:23]



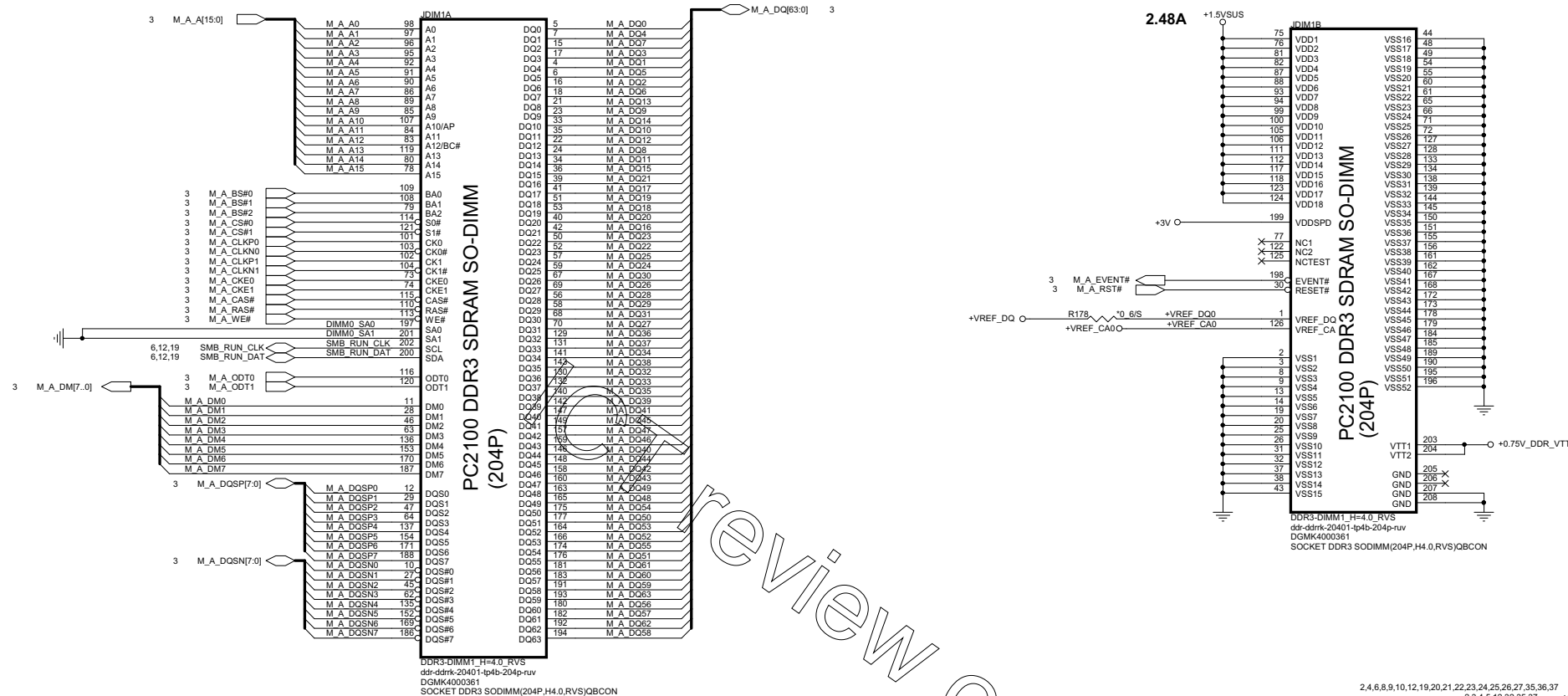
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL  DEFAULT	DISABLE ILA AUTORUN  DEFAULT	USE FC PLL  DEFAULT	USE DEFAULT PCIe STRAPS  DEFAULT	DISABLE PCI MEM BOOT  DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIe STRAPS	ENABLE PCI MEM BOOT

## FCH PWRGD

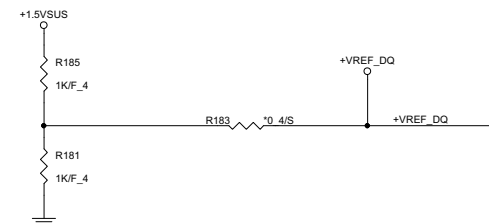
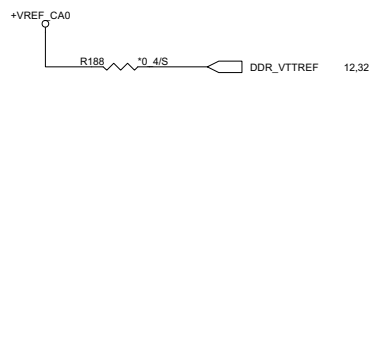
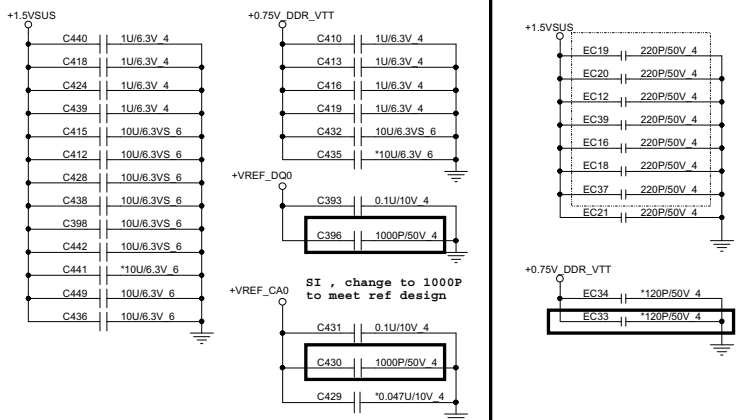


**PROJECT : U92**  
Quanta Computer Inc.

Size Custom	Document Number <b>Hudson-M3 STRAP/PWRGD</b>	Rev 1A
Date: Wednesday, March 27, 2013	Sheet 10 of 37	



## Place these Caps near So-Dimm0.

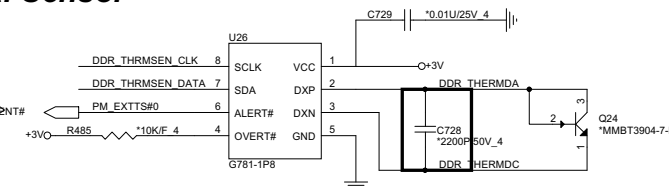
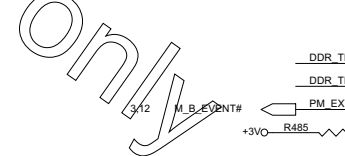


Reserved for AMD suggest



**PROJECT : U92**  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	System Memory 1/2 (5.2H)	1A
Date: Wednesday, March 27, 2013	Sheet	11 of 37



If use internal thermal IC, C9007 use 0ohm.



1

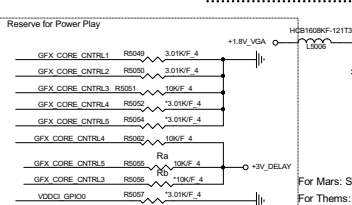
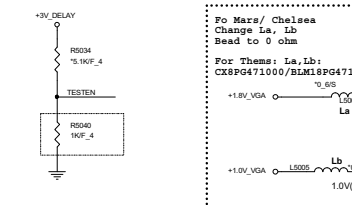
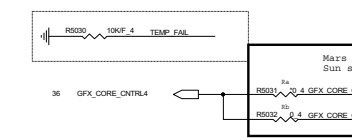
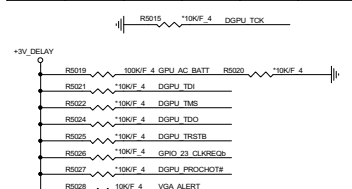




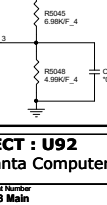
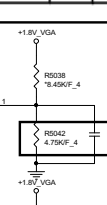
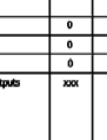
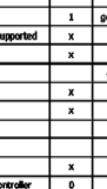
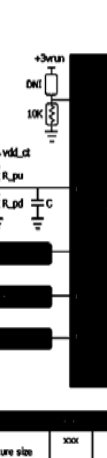
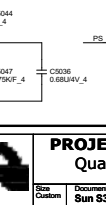
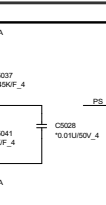
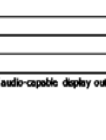
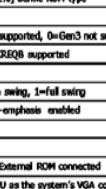
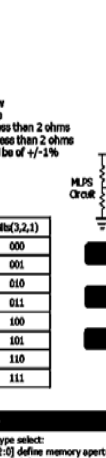
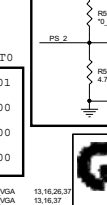
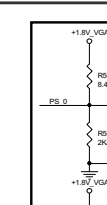
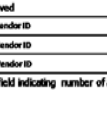
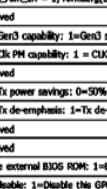
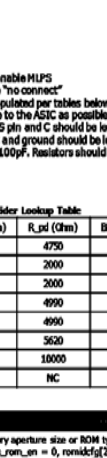
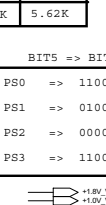
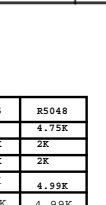
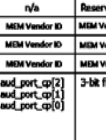
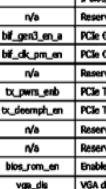
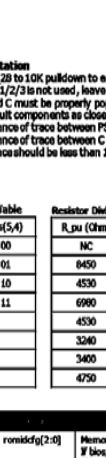
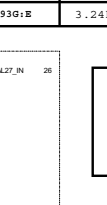
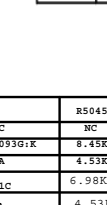
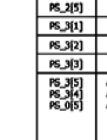
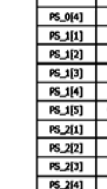
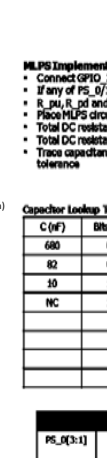
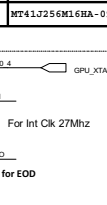
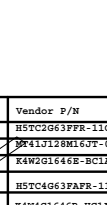
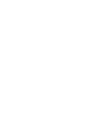
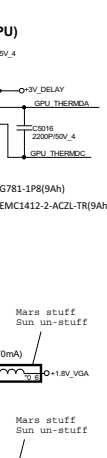
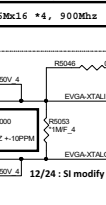
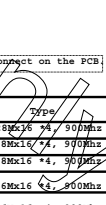
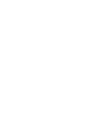
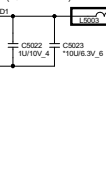
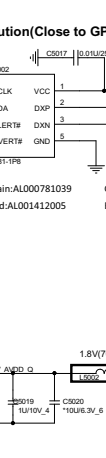
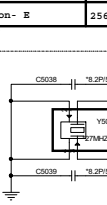
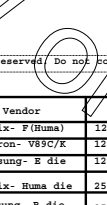
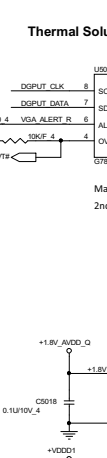
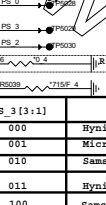
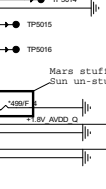
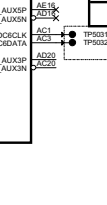
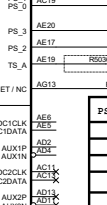
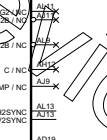
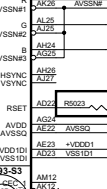
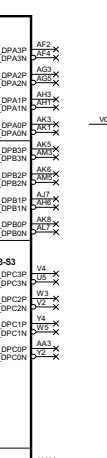
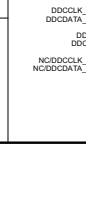
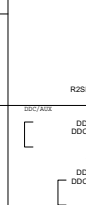
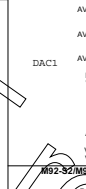
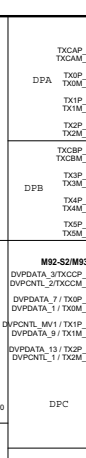
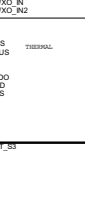
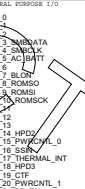
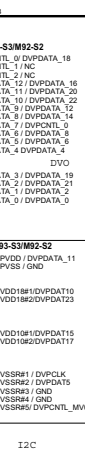
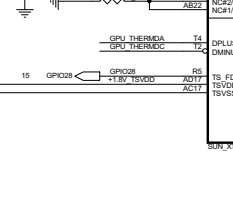
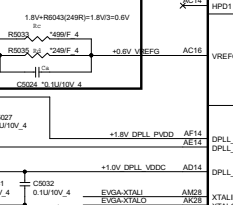
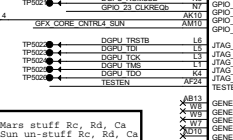
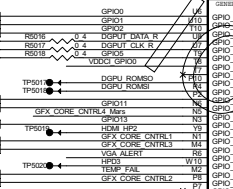
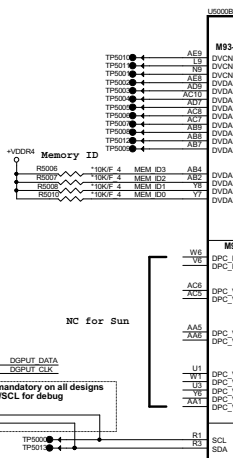
GPIO10	GPIO30	GPIO16	GPIO20	GPIO15	Sun S3
PWRCTRL5	PWRCTRL4	PWRCTRL3	PWRCTRL2	PWRCTRL1	V-CORE
0	1	1	0	1	1.175V
0	1	1	1	0	1.150V
0	1	1	1	1	1.125V
0	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Default

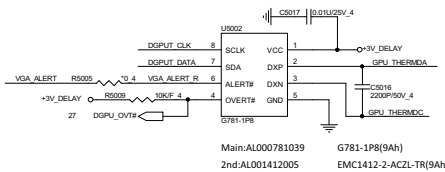
Access to SMBus and SDA/SCL is mandatory on all designs  
Add test points on SMBus and SDA/SCL for debug



For Mars: Stuff Ra only=> VDDC 1.1V  
For Thems: Stuff Ra, Rb=> VDDC 1.0V



## Thermal Solution(Close to GPU)



Main:AL000781039  
2nd:AL001412005

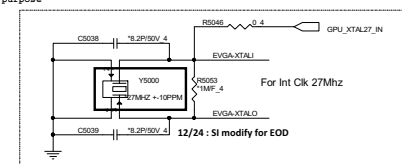
- MPS Implementation**
- Connect GPIO\_28 to 10K pulldown to enable MPS
  - If any of PS\_0/1/2/3 is not used, leave "No connect"
  - R<sub>ps</sub>, R<sub>pd</sub> and C<sub>ps</sub> must be properly populated per tables below
  - Place MPS circuit components as close to the ASIC as possible
  - Total DC resistance of trace between PS pin and C should be less than 2 ohms
  - Total DC resistance of trace between C and ground should be less than 2 ohms
  - Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

C (pF)	R <sub>ps</sub> (Ohm)
680	00
82	01
10	10
NC	11

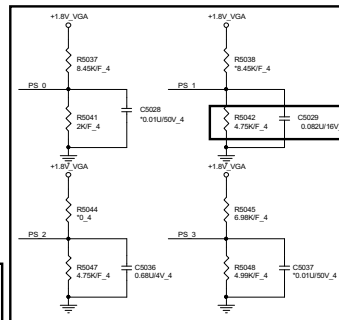
R <sub>ps</sub> (Ohm)	R <sub>pd</sub> (Ohm)	Bits(3,2,1)
NC	4750	000
4500	2000	001
4530	2000	010
6900	4900	011
4530	4950	100
3340	5620	101
3400	10000	110
4750	NC	111

PS_3[3:1]	romidk[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidk[2:0] define memory aperture size If bios_rom_en = 1, romidk[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genk_vsync
PS_1[1]	blf_gen3_en	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	blf_clk_pm_en	PCIe CLK PM capability: 1=CLKREQ supported	x	gpio_8
PS_1[3]	n/a	Reserved		genk_clk
PS_1[4]	tx_pwm_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_desamp_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dbl	VGA double: 1=Disable the GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5] PS_3[4] PS_3[0]	aud_port_cp[2] aud_port_cp[1] aud_port_cp[0]	3-bit field indicating number of audio-capable display outputs	xxx	n/a

PS_3[3:1]	Vendor	Temp	Vendor P/N	R5045	R5048
000	Hylix - F (Huma)	128Mx16 #4, 900Mhz	H5TC3G63FPR-11C	NC	4.75K
001	Micron - V89C/R	128Mx16 #4, 910Mhz	H743J128M163E-0939:E	8.45K	2K
010	Samsung - E die	128Mx16 #4, 900Mhz	K4W2G1646B-BC1A	4.53K	2K
011	Hylix - Huma die	256Mx16 #4, 900Mhz	H5TC4G63FAFB-11C	6.98K	4.99K
100	Samsung - B die	256Mx16 #4, 900Mhz	K4W4G1646B-BC1A	4.53K	4.99K
101	Micron - E	256Mx16 #4, 900Mhz	MT41J256M16HA-0939:E	3.24K	5.62K

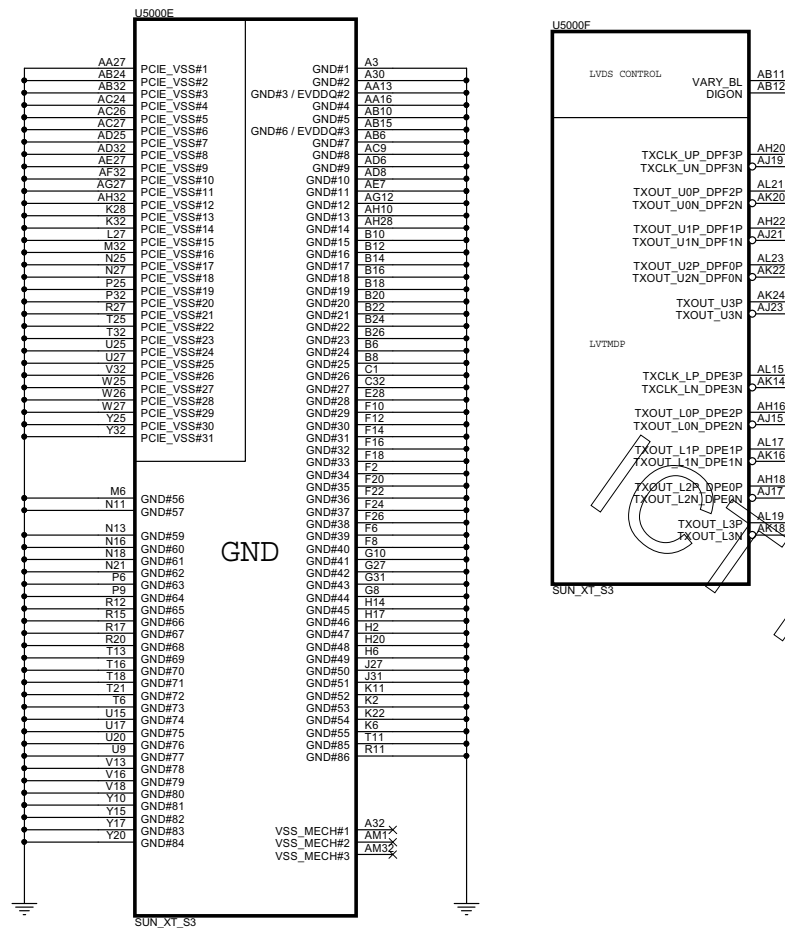


BITS => BIT0  
PS0 => 11001  
PS1 => 01000  
PS2 => 00000  
PS3 => 11000



**PROJECT : U92**  
**Quanta Computer Inc.**

Rev	Document Name	Rev
01	Sun S3 Main	01



### CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS  
0= DO NOT INSTALL RESISTOR  
1= INSTALL 3K RESISTOR  
X= DESIGN DEPENDANT  
NA= NOT APPLICABLE

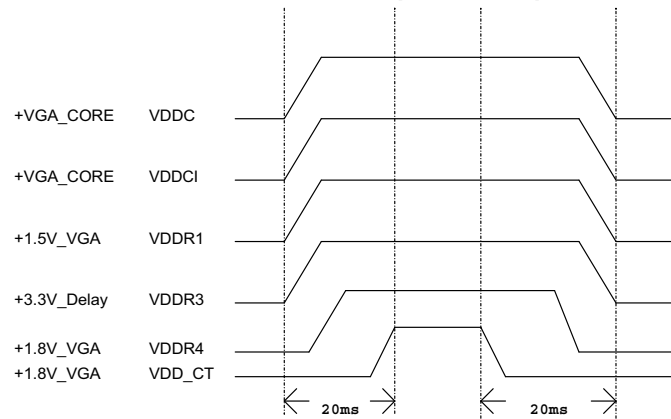
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPI00	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPI01	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPI02	RESERVED	0
RSVD	GPI08	RESERVED	0
BIF_VGA_DIS	GPI09	VGA ENABLED	0
RSVD	GPI021	RESERVED	0
BIOS_ROM_EN	GPI0_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPI0{13:11}	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on SeymourWhistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSXNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

### NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPI021 H2SYNC GENERICC GPI08 GPI02

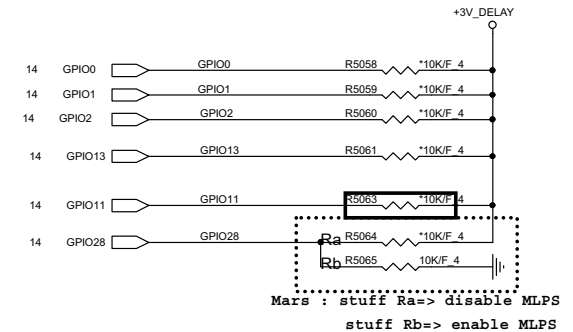
### Power Up/Down Sequence



### Memory Aperture size(Seymour)

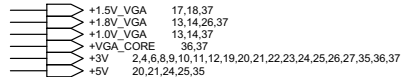
GPI09 BIOSROM		GPI013 ROMIDCFG2	GPI012 ROMIDCFG1	GPI011 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS\_ROM\_EN is set to 0.



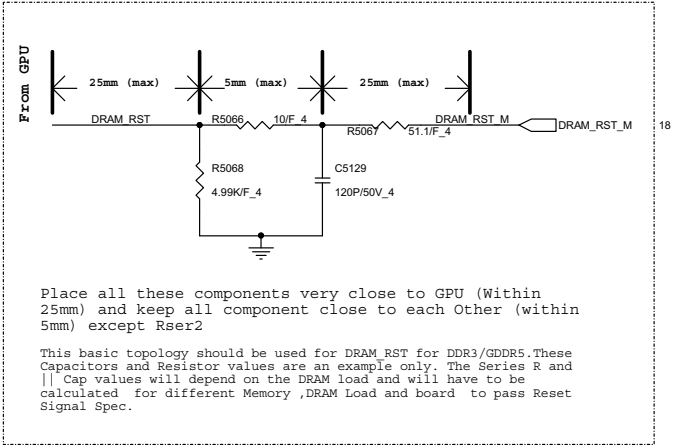
**PROJECT : U92**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	Sun S3 GND / LVDS/ Straps	1A
Date: Wednesday, March 27, 2013	Sheet 15 of 37	



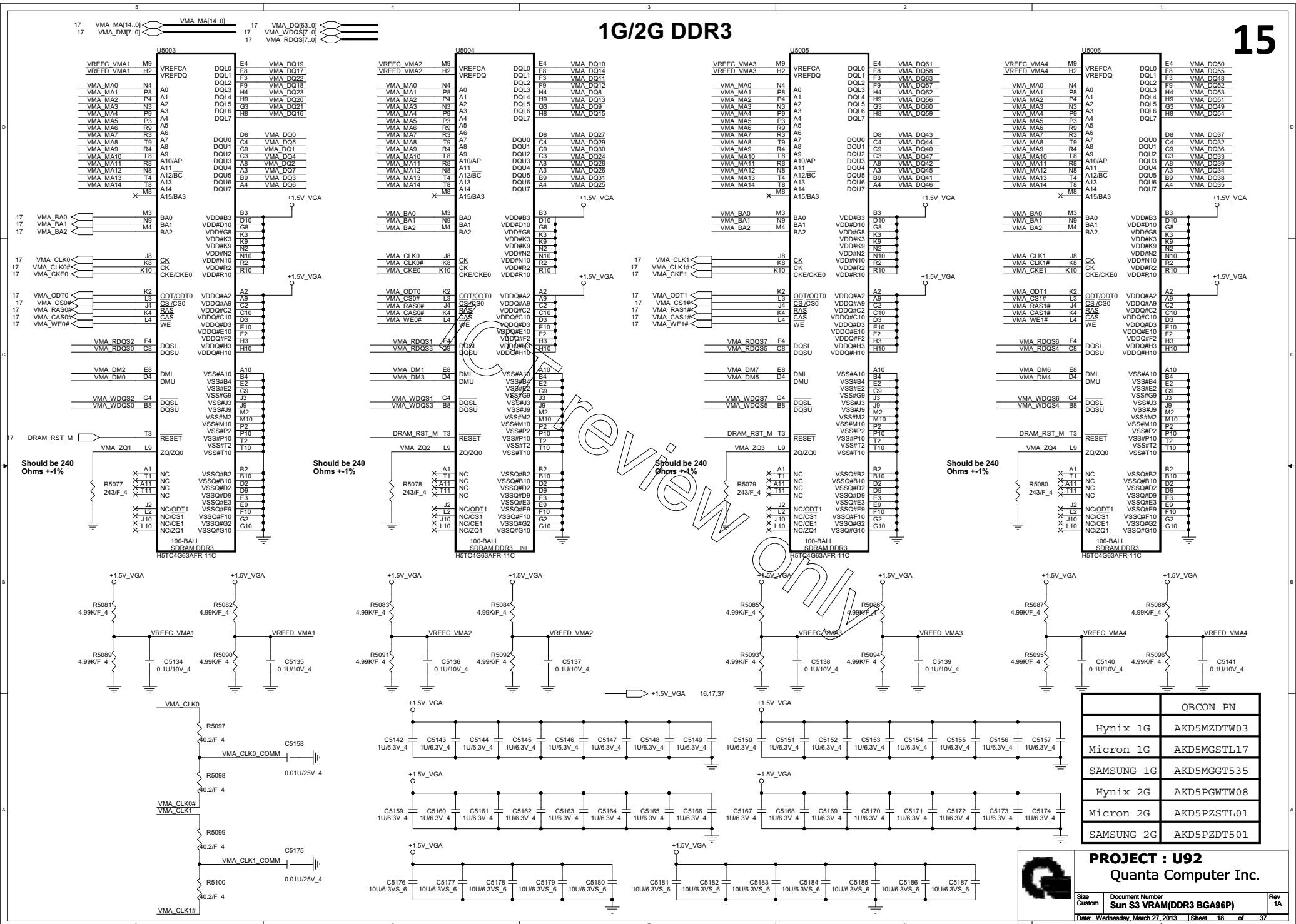
Size Custom	Document Number <b>Sun S3 Power_and_NC</b>	Rev 1A
Date: Wednesday, March 27, 2013		Sheet 16 of 37

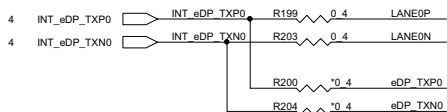




## 1G/2G DDR3

15



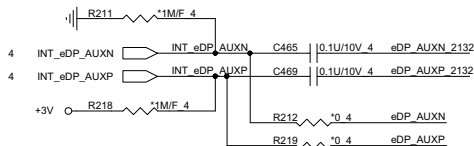


To LVDS Converter

From LVDS Converter

To eDP

From APU

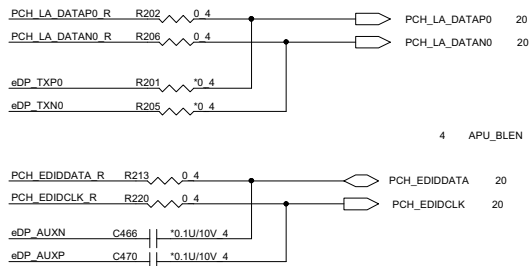


To LVDS Converter

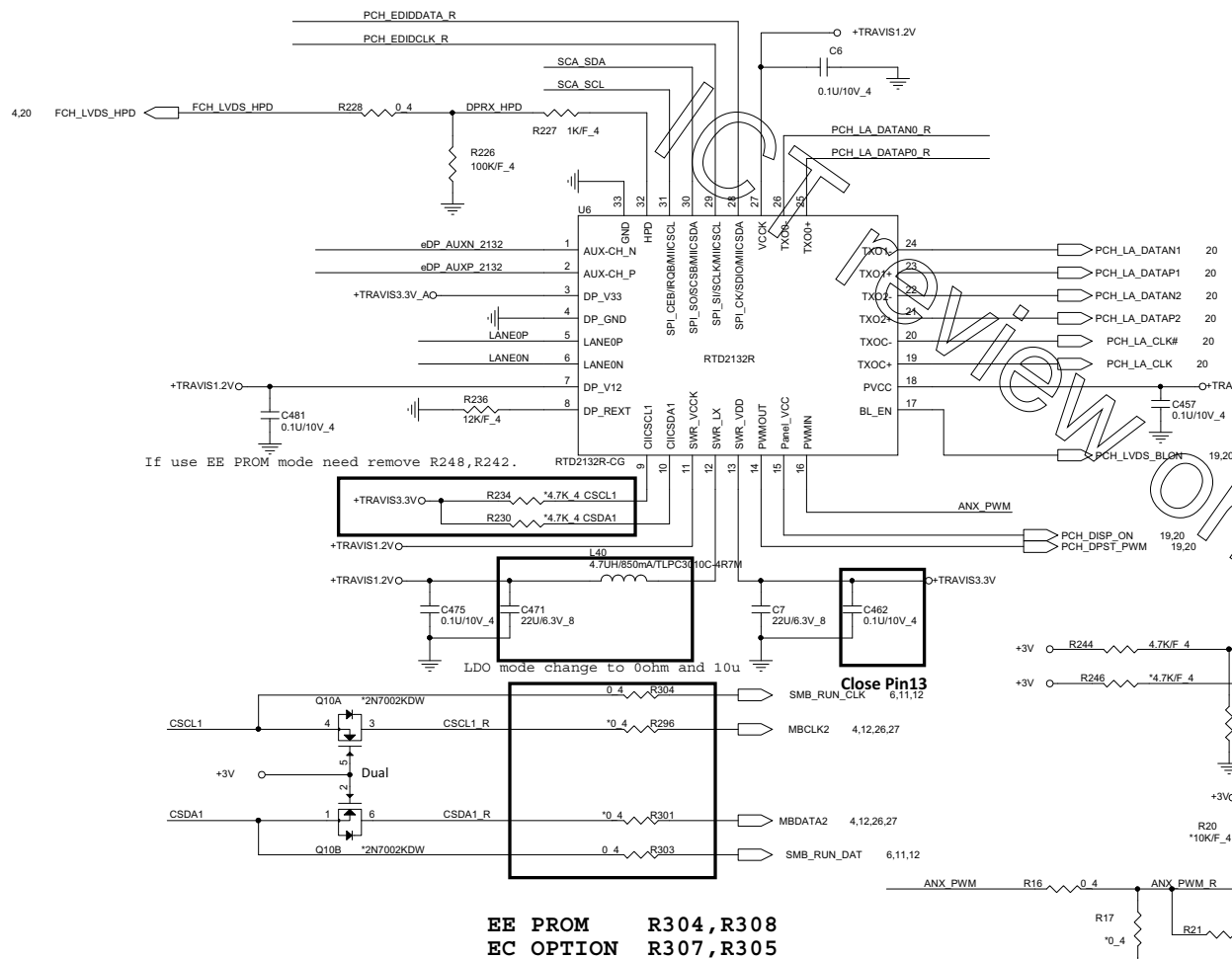
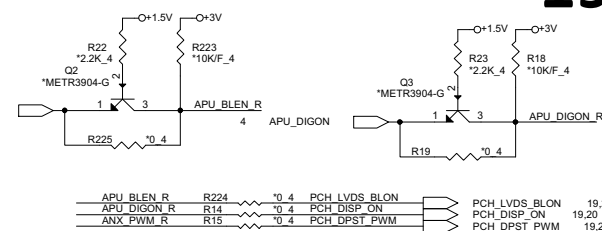
From LVDS Converter

To eDP

From APU

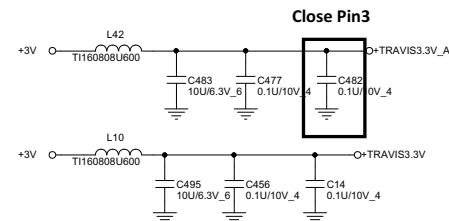


From APU

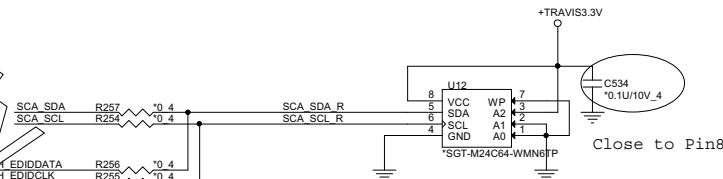


If use EE PROM mode need remove R248,R242.

EE PROM R304,R308  
EC OPTION R307,R305



Address=0xA8



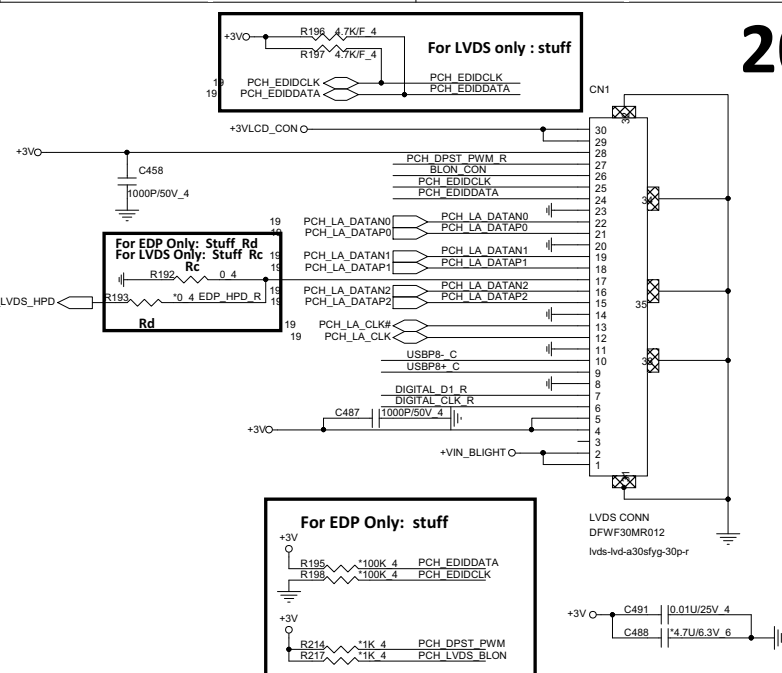
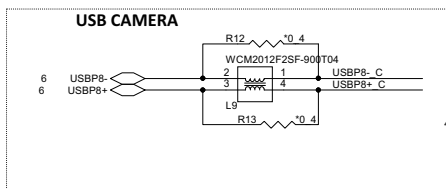
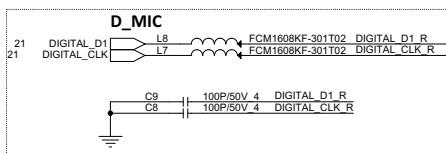
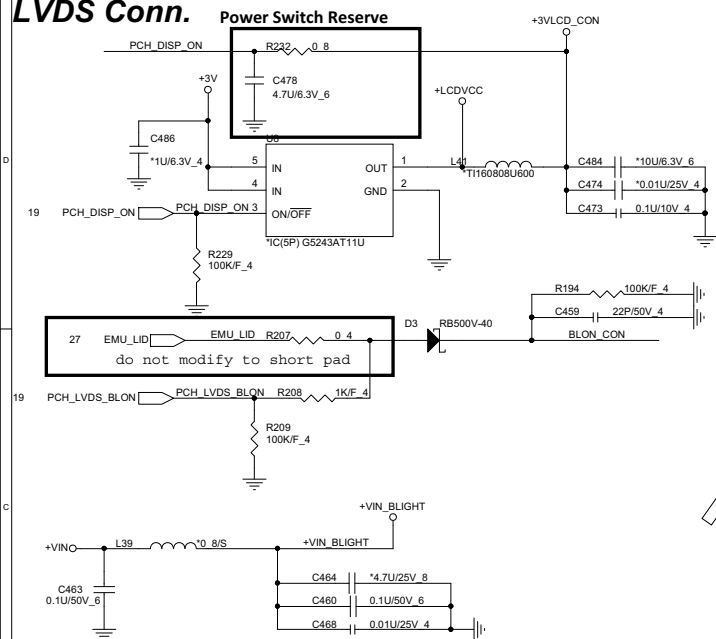
		MODE_CFG0(PIN30)	
		0	1
MODE_CFG1(PIN31)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE



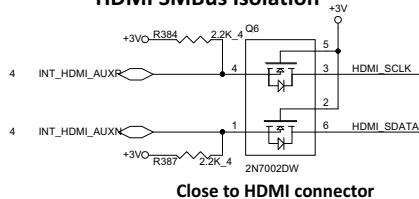
**PROJECT : U92**  
**Quanta Computer Inc.**

Size Custom Document Number  
**RTD2132S** Rev 1A  
Date: Wednesday, March 27, 2013 Sheet 19 of 37

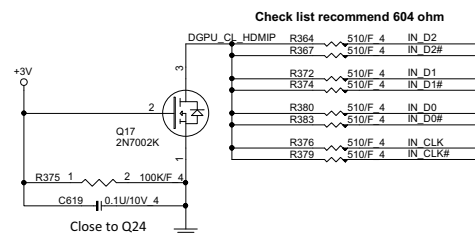
### Power Switch Reserve



## HDMI SMBus Isolation

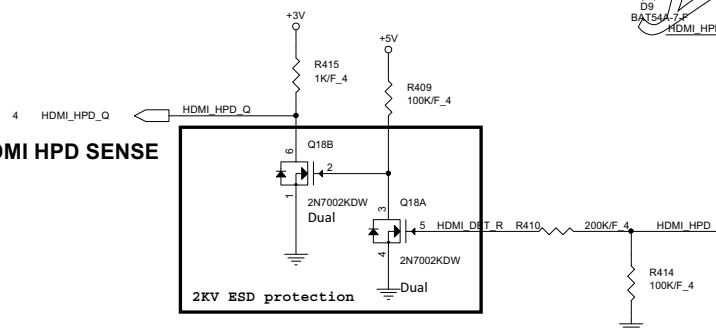


**Close to HDMI connector**

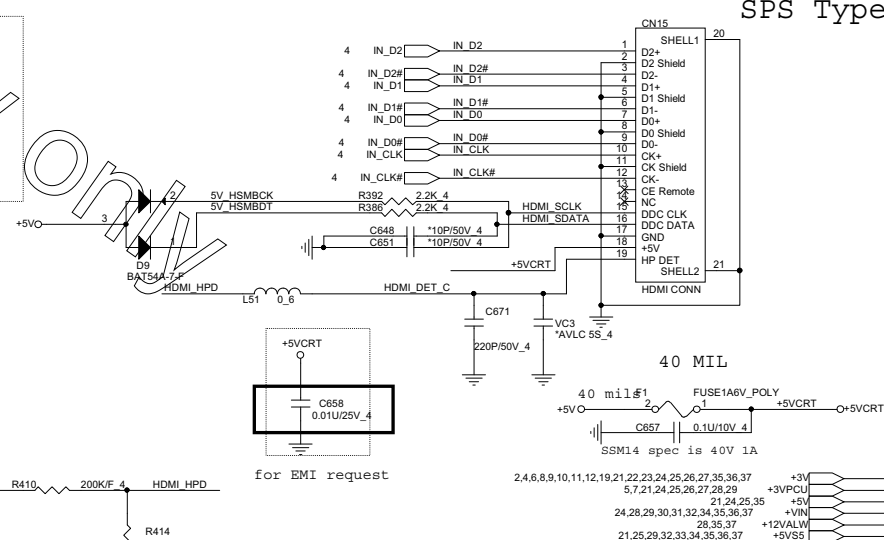
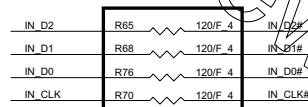


**Check list recommend 604 ohm**

## HDMI HPD SENSE



## EMI Solution

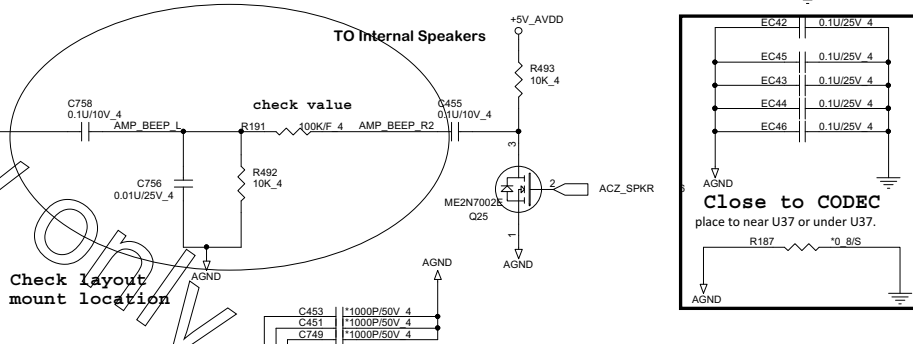
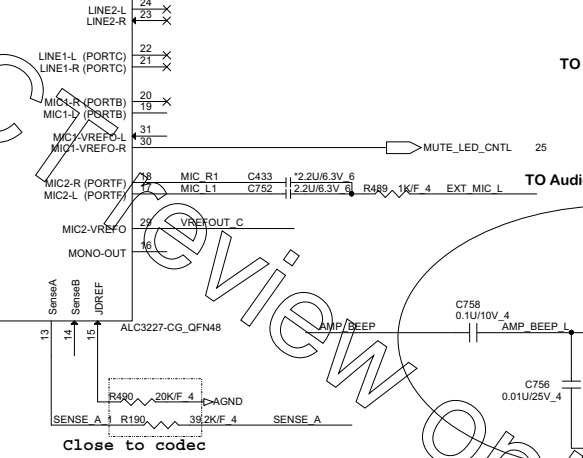
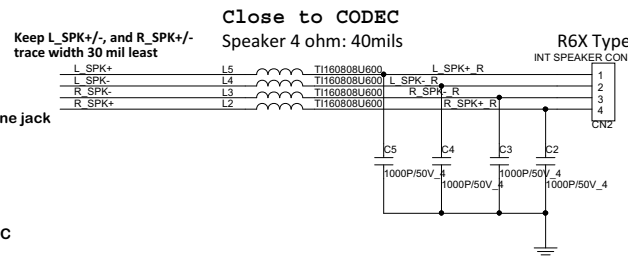
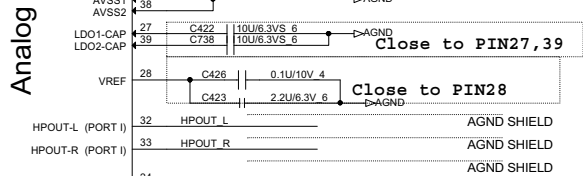
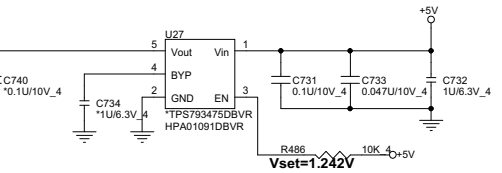


SPS Type

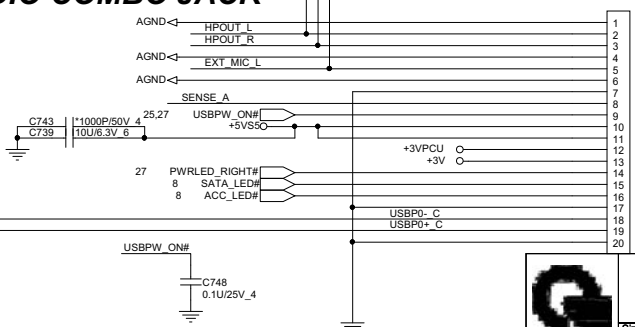
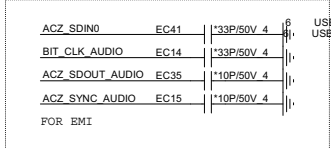


**PROJECT : U92**  
Quanta Computer Inc.

Size Custom	Document Number <b>LCD Connector (LVDS)</b>	Rev 1A
Date: Wednesday, March 27, 2013		Sheet 20 of 37

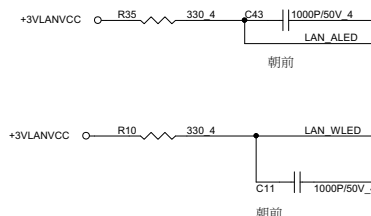
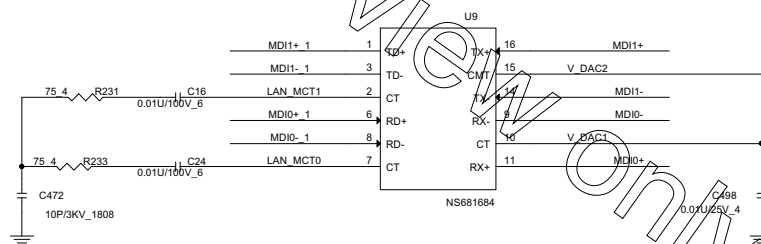
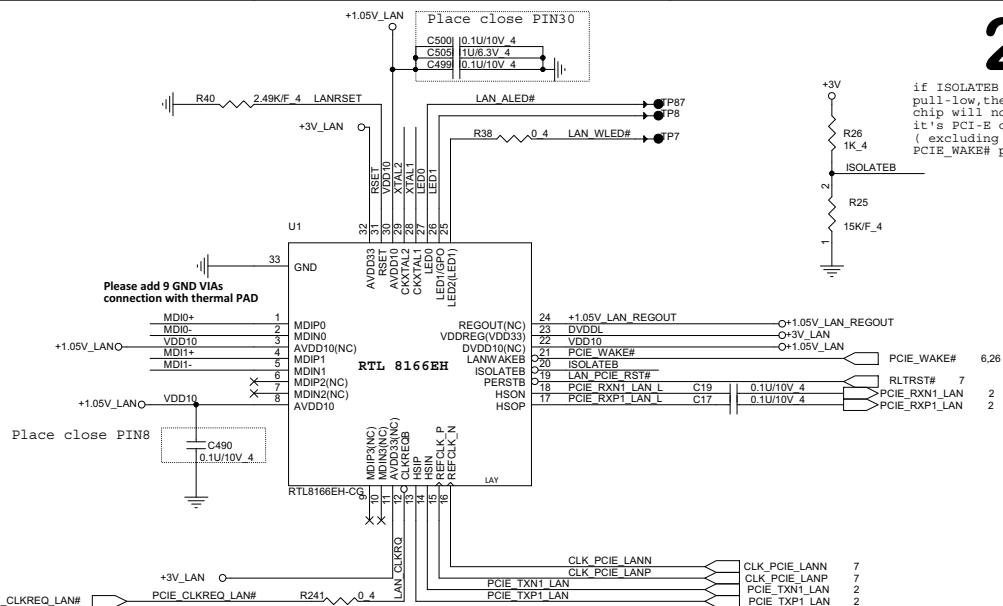


Check layout  
mount location

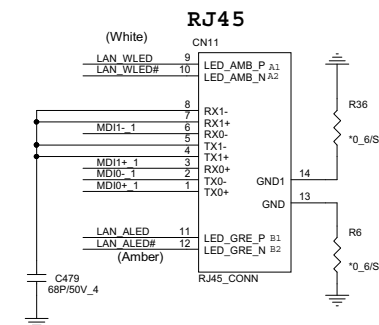


**PROJECT : U92**  
Quanta Computer Inc.

+3V  
+3VLAVCC



**LAN conn**      TWD   Type



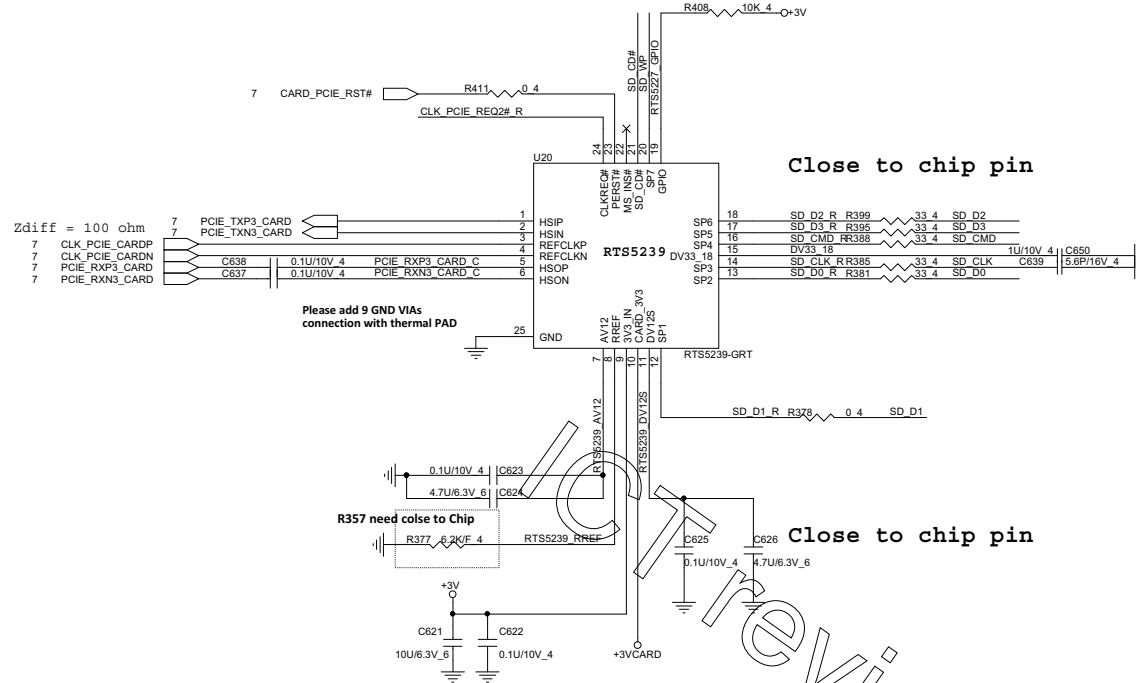
**PROJECT : U92**  
Quanta Computer Inc.

Size Custom	Document Number <b>RTL 8166EH/RJ45</b>	Rev 1A
Date: Wednesday, March 27, 2013		Sheet 22 of 37

```

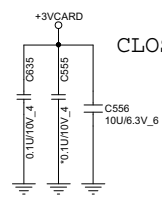
6  CLK_PCIE_REQ2#  CLK_PCIE_REQ2# R412 *0 4/S CLK_PCIE_REQ2# R

```

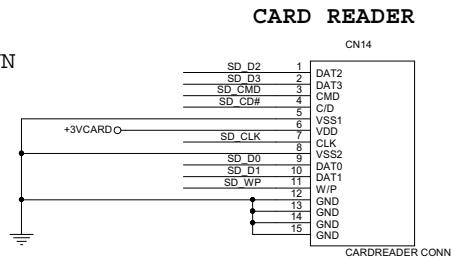


Close to chip pin

6 Close to chip pin

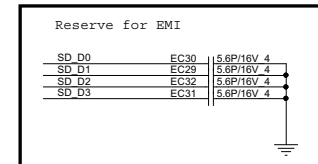


CLOSE CONN



CARD READER

R3X Type



Reserve for EMI



**PROJECT : U92**  
Quanta Computer Inc.

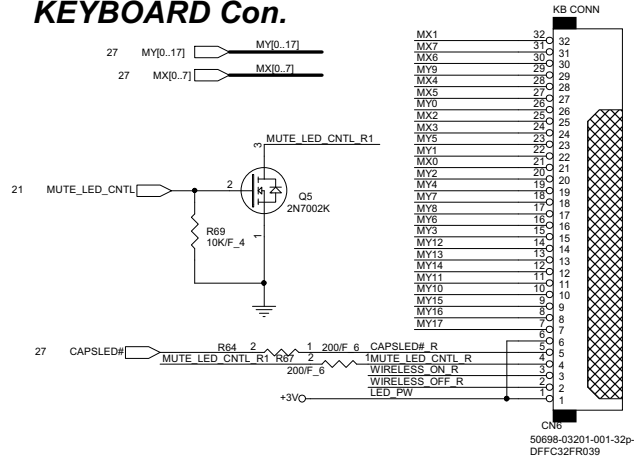
Size Custom	Document Number <b>RTS5239 &amp; CR SOCKET</b>
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Date: Wednesday, March 27, 2013	Sheet 23 of 37
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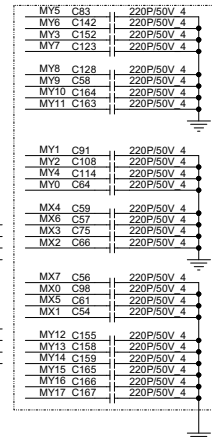
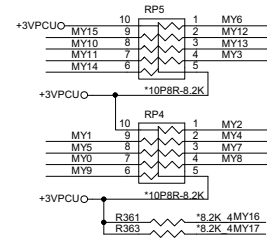


## KEYBOARD Con.

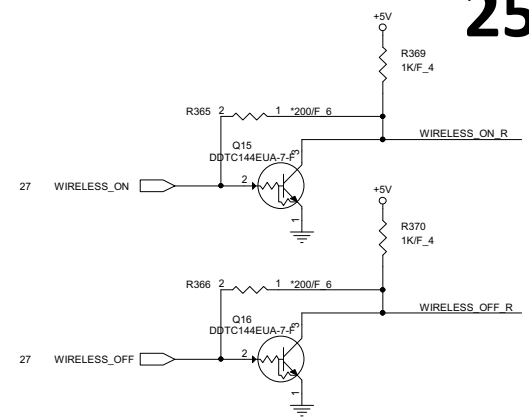


R6X Type

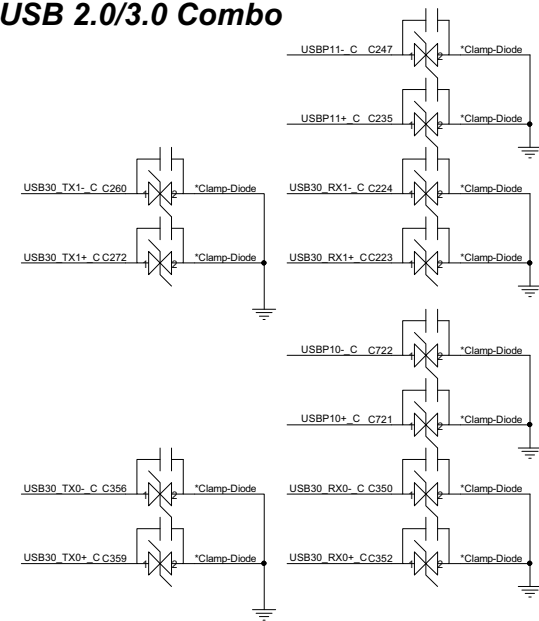
## KEYBOARD PULL-UP



25

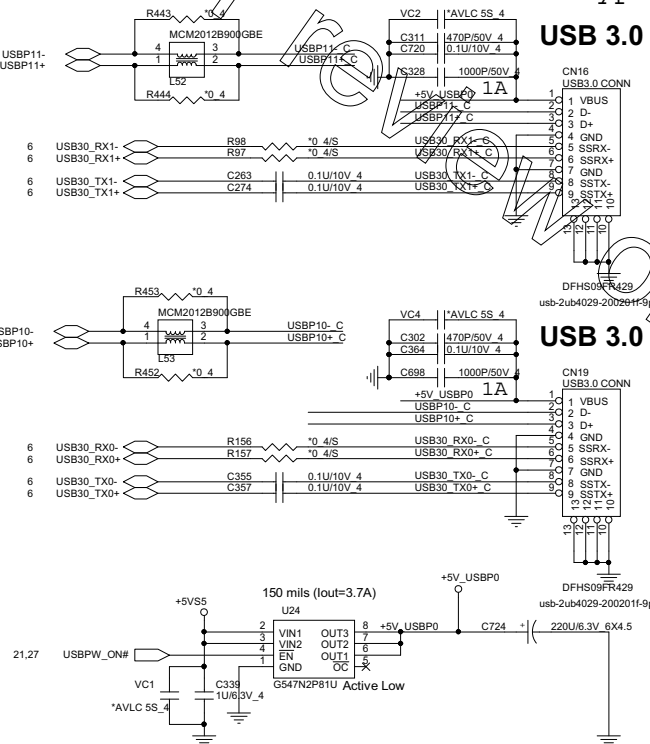


## USB 2.0/3.0 Combo

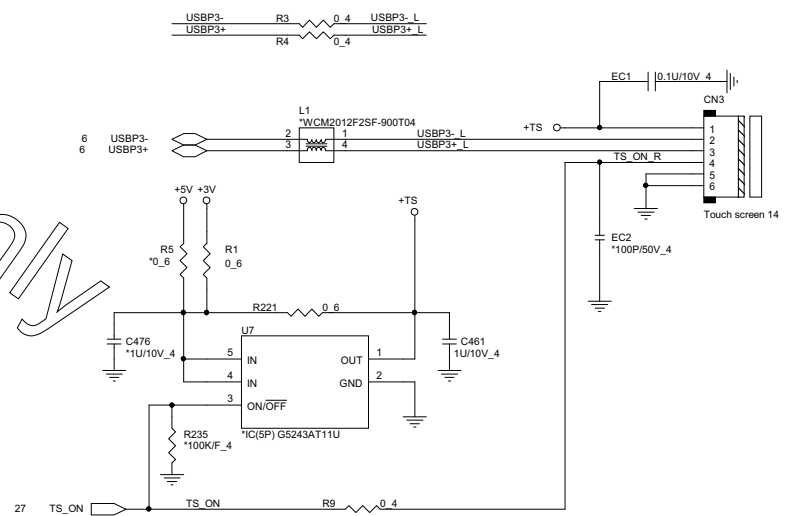


## SPS Type

### USB 3.0



## Touch screen

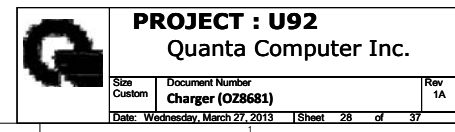


**PROJECT : U92**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	USB 3.0/KB/Green CLK	1A
Date: Wednesday, March 27, 2013	Sheet	25 of 37



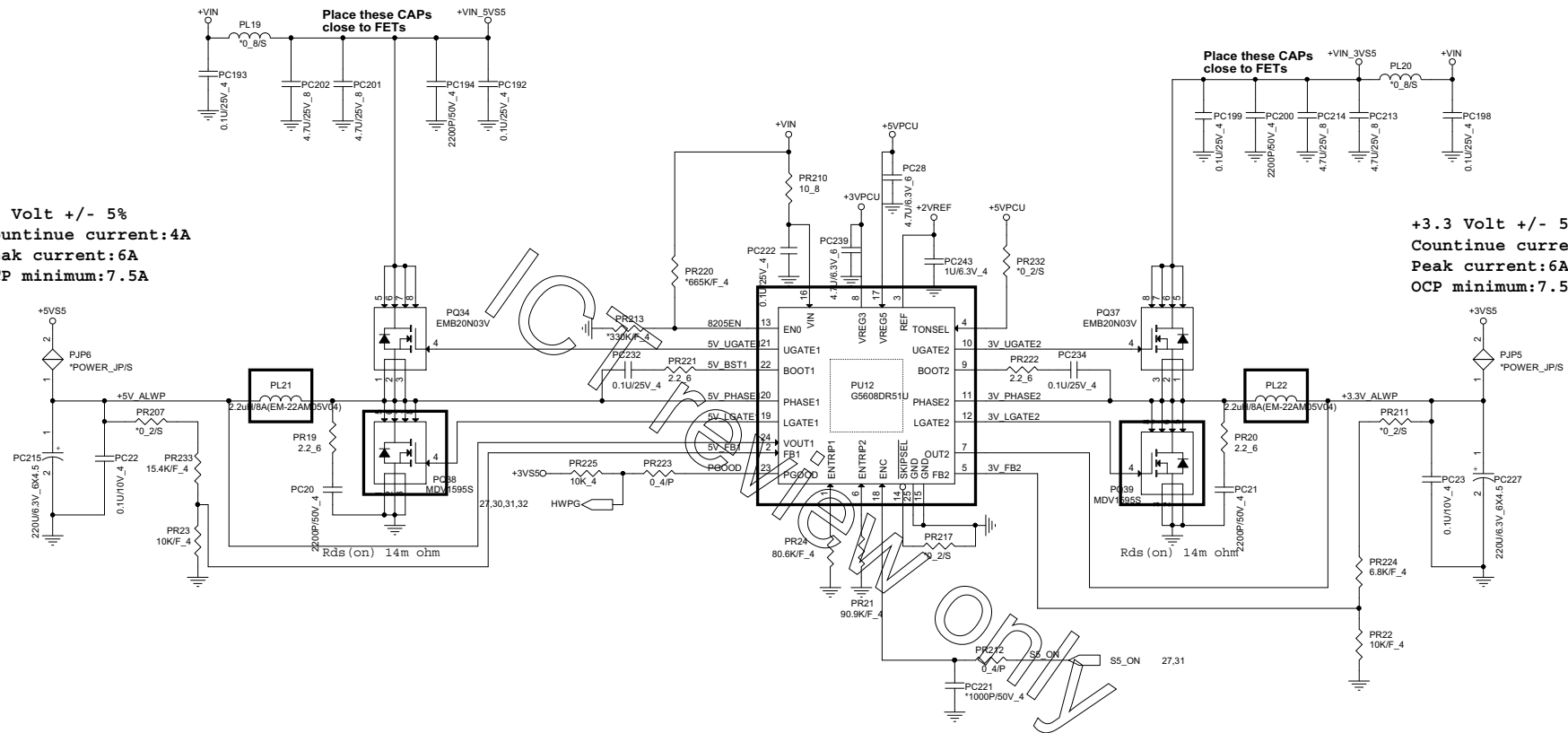




DC/DC +3VS5/+5VS5

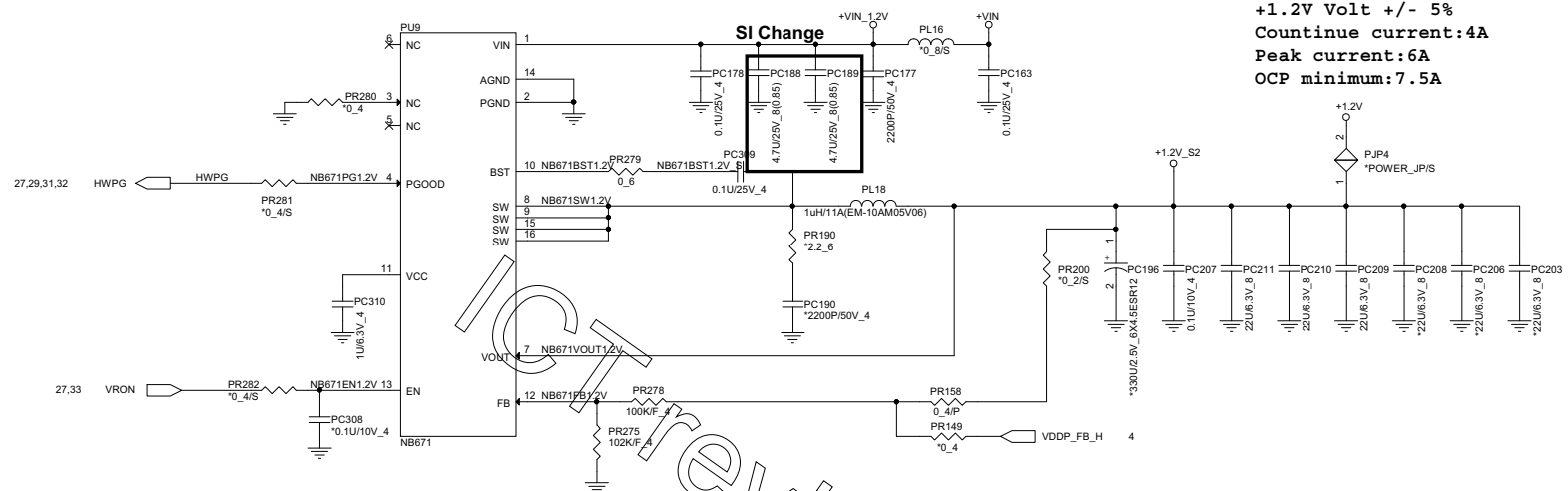
+5 Volt +/- 5%  
 Countinue current:4A  
 Peak current:6A  
 OCP minimum:7.5A

+3.3 Volt +/- 5%  
 Countinue current:4A  
 Peak current:6A  
 OCP minimum:7.5A



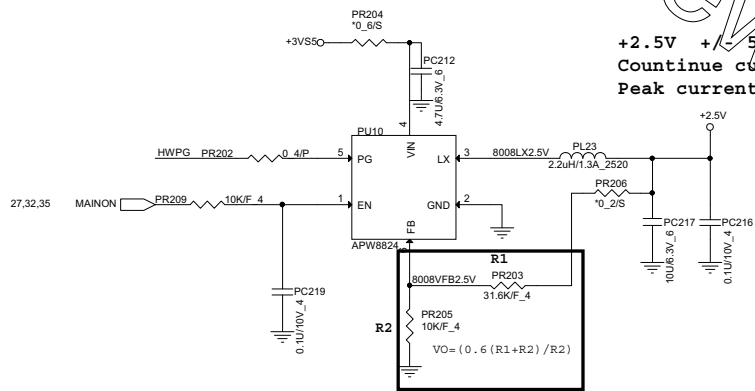
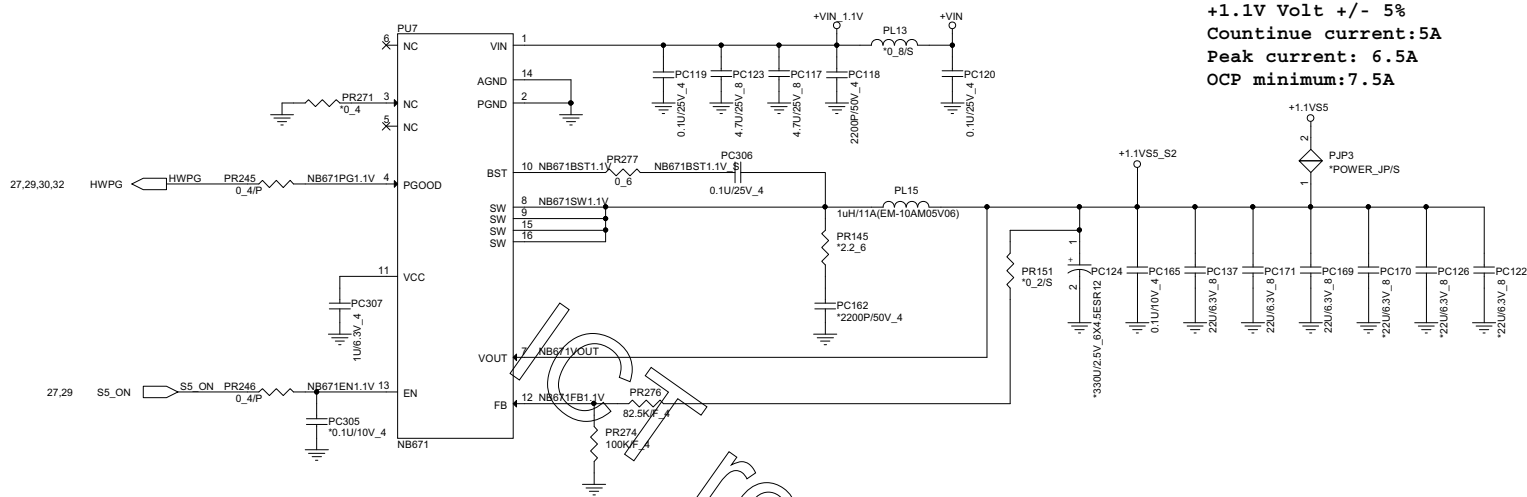
**PROJECT : R33**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>3/5VPCU(RT8223P)</b>	Rev 1A
Date: Wednesday, March 27, 2013   Sheet 29 of 37		



**PROJECT : U92**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	<b>+1.2V (RT8228)</b>	1A
Date: Wednesday, March 27, 2013 Sheet 30 of 37		

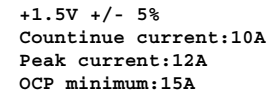


+VIN	20,24,26,29,30,32,34,35,36,37
+2.5V	5
+3VS5	6,8,9,10,26,27,29,33,35,37
+5VS5	21,25,29,32,33,34,35,36,37
+1.1VS5	9,35
+5VPCU	28,29

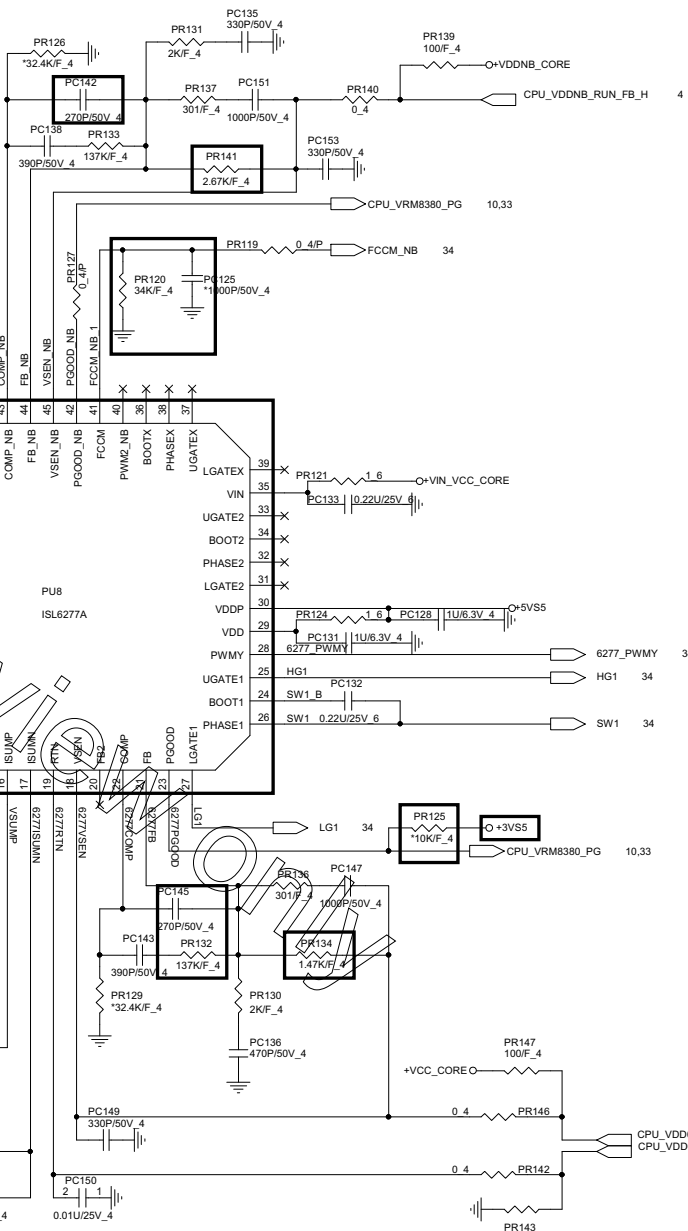
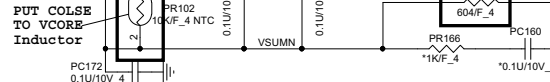
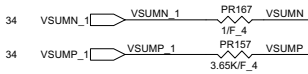
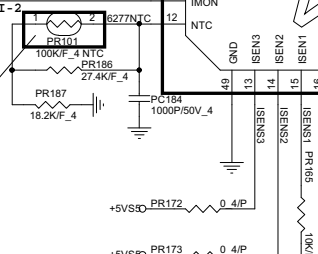
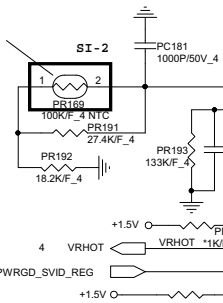
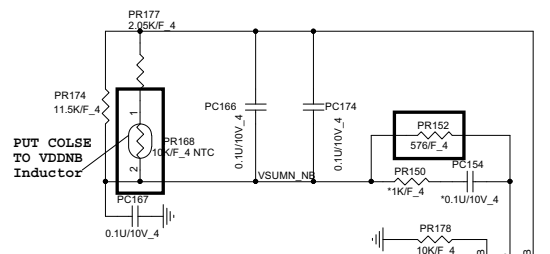


**PROJECT : U92**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	<b>+1.1VS5 (RT8228)/2.5V</b>	1A
Date:	Wednesday, March 27, 2013	Sheet 31 of 37

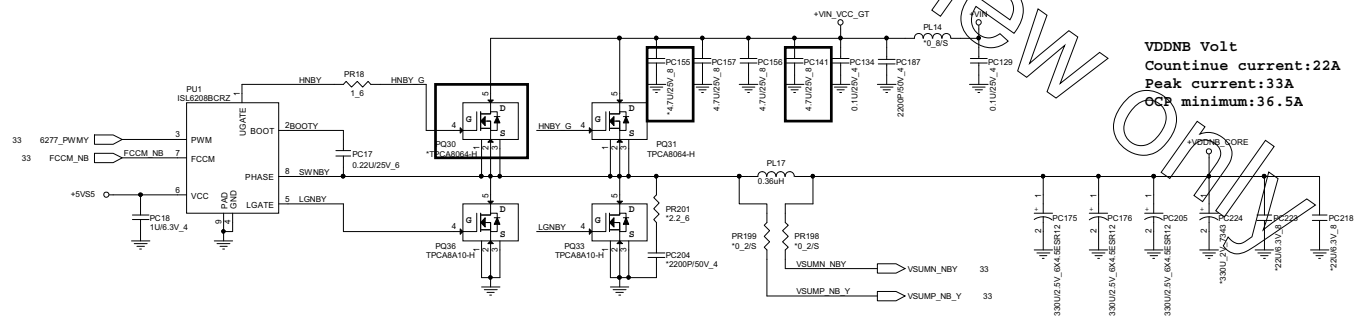
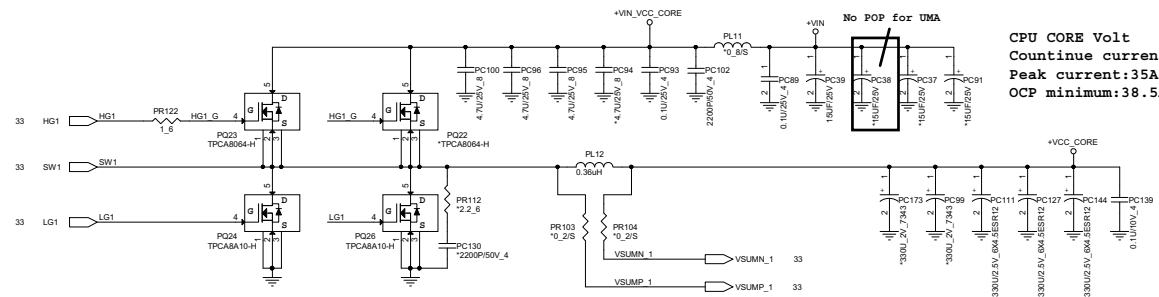






**PROJECT : U92**  
Quanta Computer Inc.

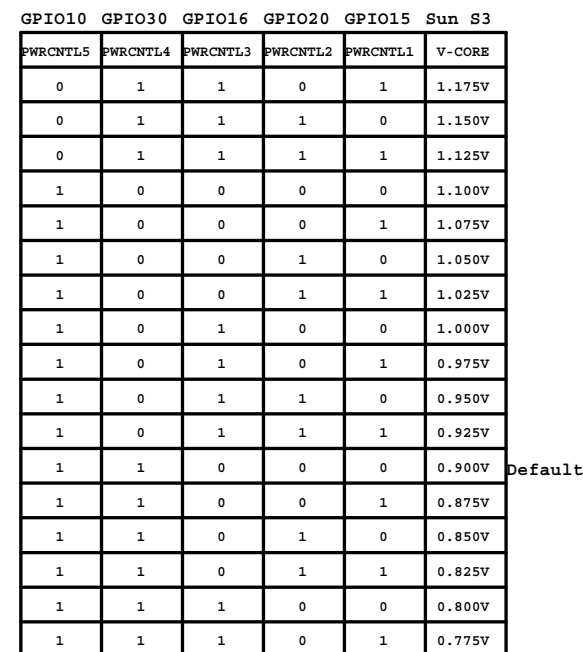
Size Custom	Document Number <b>ISL6277</b>	Rev 1A
Date: Wednesday, March 27, 2013		Sheet 33 of 37



**PROJECT : U92**  
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Size	Document Number	Rev
Custom	ISL6288	1A
Date: Wednesday, March 27, 2013   Sheet 34 of 37		





Size Custom	Document Number <b>+VGACORE NCP3218G)</b>	Rev 1.
Date:	Wednesday, March 27, 2013	Sheet 36 of 37

